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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,564	12/19/2001	Julie A. Ward	10019699-1	2164

7590 10/07/2005

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EXAMINER	
PHILLIPS, HASSAN A	
ART UNIT	**PAPER NUMBER**
2151	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,564	WARD ET AL.	
	Examiner	Art Unit	
	Hassan Phillips	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/5/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on December 19, 2001.

Information Disclosure Statement

2. The information disclosure statements filed on July 5, 2005, May 6, 2005, and December 19, 2001, have been received and considered by the Examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Peh, "The Appia topology solver".

5. In considering claims 1 and 15, Peh teaches a method and system for designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes, comprising: obtaining a design for an interconnect fabric having an interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes (page 2); identifying flow sets that traverse the interconnect device layer

(page 2); merging a pair of the flow sets thereby alleviating at least one port violation (page 2); and implementing the design (pages 2-4).

6. In considering claims 2 and 16, Peh teaches said merging adds an additional interconnect device layer to the design (page 2).

7. In considering claims 3 and 17, Peh teaches repeatedly performing, prior to said implementing, identifying an interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes and said steps of identifying flow sets and merging a pair of the flow sets, until port violations are no longer present in the design, thereby adding one or more additional interconnect device layers to the design (page 2).

8. In considering claims 4 and 18, Peh teaches generating an arrangement of flow sets in response to a set of flow requirements for the source and terminal nodes and alleviating at least one port violation associated with the arrangement of flow sets by merging a pair of the flow sets in the arrangement (pages 2-4).

9. In considering claims 5 and 19, Peh teaches inserting a dummy node into the interconnect device layer for each link that traverses the interconnect device layer and that is not terminated in the interconnect device layer (page 2).

10. In considering claims 6 and 20, Peh teaches determining for each source and terminal node one or more port violations including a number by which a set of ports for the corresponding flow sets exceed a set of available ports (pages 2-4).

11. In considering claims 7 and 21, Peh teaches said merging a pair of the flow sets alleviates at least one port violation of a source or terminal node for which the number is highest (pages 2-4).

12. In considering claims 8 and 22, Peh teaches said merging a pair of the flow sets alleviates at least one port violation of a source or terminal node for which the number is highest and also alleviates at least one port violation of a source or terminal for which the number is next highest (pages 2-4).

13. In considering claims 9 and 23, Peh teaches said step of merging a pair of the flow sets alleviates at least one port violation of a source or terminal node for which the number is highest and for which the step of merging imposes a least cost or greatest cost savings (pages 2-4).

14. In considering claims 10 and 24, Peh teaches cost is based on a cost of an interconnect device that carries the pair of flow sets (page 4).

15. In considering claims 11 and 25, Peh teaches said merging a pair of the flow sets comprises selecting pair by determining feasibility of merging the pair (pages 2-4).

16. In considering claims 12 and 26, Peh teaches said determining feasibility comprises determining whether an available interconnect device has sufficient bandwidth to carry the pair of flow sets (pages 2-4).

17. In considering claims 13 and 27, Peh teaches determining whether an available interconnect device has enough ports to carry the pair of flow sets (pages 2-4).

18. In considering claims 14 and 28, Peh teaches the interconnect fabric comprises a storage area network (pages 1-4).

19. In considering claim 29, Peh teaches a method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes, comprising: obtaining a design for an interconnect fabric having an interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes (page 2); and repeatedly forming a next interconnect device layer adjacent to either the set of source nodes or terminal nodes, thereby adding interconnect device layers to the design, until the design satisfies a set of flow requirements between the source nodes and terminal nodes without port violations, (page 2).

20. In considering claim 30, Peh teaches each added interconnect device layer reduces a number of port violations by at least one, thereby each added interconnect device layer progresses the design toward a condition of having no port violations (page 2).

21. In considering claim 31, Peh teaches said step of forming comprises identifying flow sets that traverse the interconnect device layer and merging a pair of the flow sets thereby alleviating at least one port violation (page 2).

Double Patenting

22. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

23. Claims 1-31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26, 28-41 of

copending Application No. 09/707,227. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

('227) A system comprising a set of design information including a set of flow requirements for an the interconnect fabric; fabric design tool for designing the interconnect fabric for communication between a set of source nodes and a set of terminal nodes wherein the fabric design tool generates a design for the interconnect fabric in response to the design information by generating an arrangement of flow-sets in response to the flow requirements and determining one or more port violations in the source and terminal nodes which are associated with the arrangement of flow-sets alleviating at least one of the port violations by merging a pair of-the flow-sets, wherein the step of alleviating at least one of the port violations by merging a pair of flow sets is repeated to complete the design of the interconnect fabric.

(Current Application) A method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes, comprising: obtaining a design for an interconnect fabric having an interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes; identifying flow

sets that traverse the interconnect device layer; merging a pair of the flow sets thereby alleviating at least one port violation; and implementing the design.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hassan Phillips whose telephone number is (571) 272-3940. The examiner can normally be reached on M-F 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on (571) 272-3939. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZARNI MAUNG
SUPERVISORY PATENT EXAMINER